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DOCKET NO. 99-B-186 (STMI01-99186)
SERIAL NO. 09/591,621
PATENT

IN THE SPECIFICATION:

Please replace the paragraph bridging page 15, line 9 through page 16, line 7 of the specification as filed with the following:

Table 1 and Table 2 below illustrate exemplary contents of memory models file 260. The data in memory models file 260 specifies the relative performance advantages and disadvantages of a plurality of memory types, including static random access memory (SRAM), dynamic random access memory (DRAM), read-only memory (ROM), flash RAM (FLASH), and electronically erasable programmable read only memory (EEPROM).

Memory Type	Write Power	Refresh Power	Read Power	Area Per bit	Write Speed
SRAM	high	n/a	mid	high	fast
DRAM	low	high	mid	low	fast
ROM	n/a	n/a	low	low	n/a
FLASH	high	n/a	mid	low	slow
EEPROM	low	n/a	mid	mid	mid

TABLE 1

Memory Type	Read Speed	Erase Capability	Block Size	Area Efficiency
SRAM	fast	yes	all	high
DRAM	fast	yes	all	OK low
ROM	fast	no	all	good mid
FLASH	mid	yes	limited	OK low
EEPROM	mid	yes	limited	OK low

TABLE 2

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Please replace the paragraph bridging page 17, line 4 through page 18, line 12 of the specification as filed with the following:

Table 3 and Table 4 below illustrate an additional example of a portion of code that has been re-written by code optimizer program 240 to operate in a more efficient manner. For the original code in Table 3, it is assumed that the variable J is changed in the outer loop and is continually read and written from a conventional SRAM.

```
For (J=0; J<N; J++)
{
  For (I=0; I<M; I++)
  {
    [BLOCK OF EXECUTABLE CODE]
  }
}
```

TABLE 3

Code optimizer program 240 creates the new code in Table 4, which makes J into an array in flash RAM that is written and read in consecutive locations:

```
For (J[mem_access=0]=0; J[mem_access]<N; J[mem_access+1]=
J[mem_access]+1, mem_access++)
{
  For (I[mem_access1=0]=0; I[mem_access1]<M; I[mem_access1+1]=
I[mem_access1]+1, mem_access1++)
  {
    [BLOCK OF EXECUTABLE CODE]
  }
}
```

TABLE 4

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Mem_access and mem_access1 are now stored in the memory controller
block, not in SRAM.